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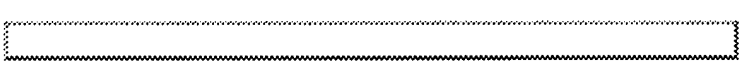
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Results 1 - 20 of 153 short listing




1 2 3 4 5 6 7 8

1 Applications of machine learning and rule induction 89%
Pat Langley , Herbert A. Simon
Communications of the ACM November 1995
Volume 38 Issue 11
Machine learning is the study of computational methods for improving performance by mechanizing the acquisition of knowledge from experience. Expert performance requires much domain-specific knowledge, and knowledge engineering has produced hundreds of AI expert systems that are now used regularly in industry. Machine learning aims to provide increasing levels of automation in the knowledge engineering process, replacing much time-consuming human activity with automatic tec ...

2 Performance and fault tolerance improvements in the Inverse Augmented Data Manipulator network 88%
Robert J. McMillen , Howard Jay Siegel
Proceedings of the 9th annual symposium on Computer Architecture April 1982
The Inverse Augmented Data Manipulator (IADM) is a multistage interconnection network based on the Augmented Data Manipulator (ADM) and Feng's data manipulator. It is designed to be used in large-scale parallel/distributed processing systems for communication among processors, memories, and other system devices. Two aspects of IADM network design are discussed: performance and fault tolerance. A single stage look-ahead scheme for predicting blockage is presented to enhance performance. Next ...

3 Poster session: A high resolution diagnosis technique for open and short defects in FPGA 87%

 interconnects
Mehdi Baradaran Tahoori
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003
A two-step diagnosis flow, coarse-grain and fine-grain, is presented in order to identify a faulty element in the FPGA interconnects. The fault models used for interconnect are open, resistive-open, and bridging fault. The coarse-grain phase identifies the faulty net, the routing between two consecutive sequential elements in the FPGA. This phase is performed by just post-processing tester results for the test configurations used for interconnect testing. During the fine-grain step, the faulty n ...

4 Knowledge based fault management for OSI networks 84%

Celia A. Joseph , A. Sherzer , K. Muralidhar
Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1 June 1990
The OSI Fault Management system (OSIFaM) is an evolving knowledge-based system for fault management of Open System Interconnection (OSI) networks. Our goal is to develop a knowledge-based tool that will reduce the expertise needed to recognize, diagnose and correct faults in OSI networks. For our first implementation, we are focusing on MAP 3.0 networks. This paper provides an overview of fault management in general, a brief survey of other fault management developments, the characteristics ...

5 Experience Using Multiprocessor Systems—A Status Report 84%

Anita K. Jones , Peter Schwarz
ACM Computing Surveys (CSUR) June 1980
Volume 12 Issue 2

6 An efficient algorithm to determine the image of a parallelepiped under a linear transformation 84%

V Visvanathan , L S Milor
Proceedings of the second annual symposium on Computational geometry August 1986
An efficient algorithm to determine the image of a parallelepiped under a linear transformation is presented. The work was motivated by certain problems in the testing of analog integrated circuits. The method is based on specifying the boundary hyperplanes that define the image polytope and is of polynomial complexity in n (the dimension of the parallelepiped), for a fixed value of the dimension of the range of the linear transformation. The algorithm has been implemented ...

7 Cross-fertilizing FSM verification techniques and sequential diagnosis 83%

G. Cabodi , P. Camurati , F. Corno , P. Prinetto , M. Sonza Reorda
Proceedings of the conference on European design automation November 1992

8 VLSI test expertise system using a control flow model 82%

G. Saucier , C. Bellon
21st Proceedings of the Design Automation Conference on Design automation June 1984
The automatic generation of test programs for VLSI circuits and systems remains an unanswered wish. The solution seems to be a computerized expert aid, integrated in a whole system for circuit design. This paper outlines the concepts of an intelligent agent whose aims

are to help the designer in appraising the diagnosability of the device or the system under design, to suggest design modifications, to generate test patterns for elementary modules and to assemble the basic test sequences int ...

9 Novel self-test methods: A scalable software-based self-test methodology for programmable processors 82%

Li Chen , Srivaths Ravi , Anand Raghunathan , Sujit Dey

Proceedings of the 40th conference on Design automation June 2003

Software-based self-test (SBST) is an emerging approach to address the challenges of high-quality, at-speed test for complex programmable processors and systems-on chips (SoCs) that contain them. While early work on SBST has proposed several promising ideas, many challenges remain in applying SBST to realistic embedded processors. We propose a systematic scalable methodology for SBST that automates several key steps. The proposed methodology consists of (i) identifying test program templates tha ...

10 Computing curricula 2001 82%

Journal on Educational Resources in Computing (JERIC) September 2001

11 Formal verification in hardware design: a survey 82%

Christoph Kern , Mark R. Greenstreet

ACM Transactions on Design Automation of Electronic Systems (TODAES) April 1999 Volume 4 Issue 2

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

12 A management system for a PACS network in a hospital environment 82%

Viviane Jonckers , B. Criel

Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2 June 1990

The paper reports on a network management system for a Picture Archiving and Communication System (PACS) in a hospital environment. The size of a typical data transfer in this environment is several orders of magnitude larger than a typical data transfer in a local area computer network. To ensure reasonable response times to the system's users, it is necessary to sequentialise the image traffic on the PACS network. Knowledge about patient flow, radiologist flow, and image flow which is ava ...

13 Poster session: A four-bit full adder implemented on fast SiGe FPGAs with novel power control scheme 82%

K. Zhou , M. Chu , C. You , J.-R. Guo , Channakeshav , J. Mayega , B. S. Goda , R. P. Kraft , J. F. McDonald

Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

The low operating speed of current CMOS Field Programmable Gate Arrays (FPGAs), i.e.,

10-220 MHz, has prevented their use in high-speed digital applications. With the advent of IBM Silicon Germanium (SiGe) 7HP technology, designers have been able to design FPGAs operating in the gigahertz range. This paper is going to elaborate on the implementation of a 4-bit ripple-carry full adder (FA) on the new SiGe FPGA with new architectures and a novel power management strategy. The 1-bit FA can be reali ...

14 Poster session: Application-dependent testing of FPGAs for bridging faults 82%
Mehdi Baradaran Tahoori
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003
A new technique is presented for testing for bridging faults in the interconnects of an arbitrary design implemented in an FPGA. The configuration of the routing resources used in the original design remains unchanged in the test configurations. Only the logic blocks used in the design are reprogrammed in order to implement single-term functions, logic functions with only one minterm or one maxterm. As shown by formal proofs, all activated faults are detected when single-term functions and appro ...

15 Poster session: A physical retiming algorithm for field programmable gate arrays 82%
Peter Suaris , Dongsheng Wang , Pei-Ning Guo , Nan-Chi Chou
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003
In this paper, we present a physical retiming algorithm for sequential circuits implemented in field programmable gate arrays (FPGAs). This algorithm can speed up the sequential circuits by reducing delay of all critical paths with negative slacks. By taking advantage of the physical information provided by placed circuits, this algorithm integrates two operations: retiming and register duplication. Retiming moves registers across combinational components. Register duplication moves registers ac ...

16 Poster session: Design strategies and modified descriptions to optimize cipher FPGA implementations: fast and compact results for DES and triple-DES 82%
Gaël Rouvroy , Francois-Xavier Standaert , Jean-Jacques Quisquater , Jean-Didier Legat
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003
We propose a new mathematical DES description that allows optimized implementations. It also provides the best DES and triple-DES FPGA implementations known in term of ratio throughput/area, where area means the number of FPGA slices used. First, we get a less resource consuming unrolled DES implementation that works at data rates of 21.3 Gbps (333 MHz), using VIRTEX II technology. In this design, the plaintext, the key and the mode (encryption/decrytion) can be changed on a cycle-by-cycle basis ...

17 Poster session: Wireless sensor networks: a power-scalable motion estimation IP for hybrid video coding 82%
Federico Quaglio , Maurzio Martina , Fabrizio Vacca , Guido Masera , Andrea Molino , Gianluca Piccinini , Maurizio Zamboni
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003
Wireless Sensor Networks are an emerging phenomenon in the research community. The design and development of network architectures and nodes implementation are fostering many

research activities. Due to their wide application fields and pervasive employment possibilities, the investigation of novel classes of wireless sensor nodes is of great concern. In this paper we presented a novel Power-Scalable Motion Estimation IP suitable for video-surveillance over Wireless Sensor Networks. The proposed ...

18 Poster session: Lattice adaptive filter implementation for FPGA 82%

Zdenek Pohl , Rudolf Matoušek , Jirí Kadlec , Milan Tichý , Miroslav Lícko

Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

Our poster introduces an innovative RLS Lattice filter implementation for FPGAs. The signal processing applications typically require wide numeric range, and that poses a problem when using an FPGA implementation. Our approach is based on arithmetic using logarithmic numeric representation (LNS). The test application - an adaptive noise canceller - has been optimized for the Xilinx Virtex devices. It consumes roughly 70% of all logic resources of the XCV800 device and all block memory cells. The ...

19 Poster session: An FPGA architecture with built-in error correction capability 82%

P. K. Lala , B. Kiran Kumar

Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

The use of very deep submicron technology makes VLSI-based digital systems more susceptible to transient or soft errors, and thus compromises their reliability. This paper proposes an FPGA architecture inspired by the human immune system that allows tolerance of transient errors. The architecture is composed of a two-dimensional array of identical functional cells with different genetic codes. These codes are chosen based on the required functions to be performed by the functional cells. An erro ...

20 Poster session: Synthetic circuit generation using clustering and iteration 82%

Paul D. Kundarewich , Jonathan Rose

Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

The development of next-generation CAD tools and FPGA architectures requires benchmark circuits to experiment with new algorithms and architectures. There has always been a shortage of good public benchmarks for these purposes, and even companies that have access to proprietary customer designs could benefit from designs that meet size and other particular specifications. In this paper, we present a new method of generating realistic synthetic benchmark circuits to help alleviate this shortage. ...

Results 1 - 20 of 153 short listing

Prev Page 1 2 3 4 5 6 7 8 Next Page

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